Past and future of InP-based photonic integration

Meint Smit

Acknowledgements: The COBRA team NWO, EU-IST program, STW, IOP







Technische Universiteit **Eindhoven** University of Technology

Where innovation starts

COBRA

Communication Technologies: Basic Research and Applications

COBRA staff

- ~25 scientific staff & technicians
- ~25 postdocs
- ~50 PhD

Core

- Materials (HGF)
- Components (OED)
- Systems (ECO)

Other

- Radio Communications (CWSe)
- Electromagnetics (EM)
- Micro Electronics (MsM)
- Signal Processing (SPS)
- Functional Materials

800 m² cleanroom







Technische Universiteit Eindhoven University of Technology

Outline

- The Past / Moore's law in Photonics
- The Future / 1 Generic Integration Technology
- The Future / 2 Nanophotonic Integration Technology



Moore's law for WDM PICs



Photonic Integration

AWG demultiplexer

Meint Smit, Electronics Letters 1988



Photonic Integration

UCSB, 7 Nov 2008 5/31



COBRA TU/e Technische Universiteit Eindhoven University of Technology

Example of Photonic IC: 4λ **OXC**

Herben, PTL, 1999



Photonic Integration

UCSB, 7 Nov 2008 6/31



TU/e Technische Universiteit Eindhoven University of Technology

40-wavelength digitally tunable laser



OPT ++

16-channel PHASAR wavelength selector



- 100-GHz channel spacing
- Crosstalk < -35 dB
- Zero-loss operation
 @ 50 mA for all channels





R. Mestric et al, OFC'2000, March 2000, Baltimore

Groupement d'Intérêt Economique

1-out-of-64 WDM channel selector (N.Kikuchi, EL, 2002)



(chip size : $7.0 \ge 7.0 \ge 7.0 = 200$

Today's technology for WDM integration: World's smallest integrated AWGs: 40 channels integrated



May 2004

Towards LSI: Infinera WDM circuits





TU

e

Moore's law for WDM PICs



What went wrong?

- Since 1990 worldwide more than 1 B\$ invested in development of integration technologies
- Almost all research was application driven
- Therefore almost as many technologies as applications
- For most of them: market too small for payback of investments
- (By far too) many degrees of freedom
 - many different materials and technologies
 - many different component types
 - many different wavelength ranges and applications







The (only?) way out

- Develop a limited number of generic wafer-scale integration technologies, that can support a broad range of functionalities and applications
- Move to a generic foundry model (as in CMOS)
 - Convergence of technologies
 - Decouple design (IP) from technology (IP)
 - Set up libraries and tools for ASPIC design
 - Organize training and design support for fabless users
- Work on market development (new applications)







Outline

- The Past / Moore's law in Photonics
- The Future / 1 Generic Integration Technology
- The Future / 2 Nanophotonic Integration Technology



Generic Integration philosophy







Photonic Integration with 3 basic building blocks (BB)



Examples



optical crossconnect



optical crossconnect



wavelength converter





WDM-TTD switch Cascaded WDM laser



tunable multiwavelength laser



picosecond pulse laser



multiwavelength laser



WDM ring laser



Photonic Integration

UCSB, 7 Nov 2008 18/31



New: A fast tunable AWG-laser



AWG channel spacing 100 GHz







Switch-on time: 3 ns Switch-off time: 4 ns



A Generic Integration Platform

JePPIX:

Joint European Platform for InP-based Photonic Integration of Components and Circuits

Industrial partners:	Bookham, CIP, Cedova, Alcatel-Thales III-V Lab, u2t, FhG-HHI, Svedice ASML, Aixtron, OPT
Photonic CAD:	Phoenix, Photon Design, Filarete
Universities:	COBRA –TU/e, Cambridge, KTH, COM, CNRS
Coordination:	COBRA

Step 1: Small-scale access to the COBRA process for research purposes (proof-of-concept)

Step 2: Feasibility of an industrial foundry (EuroPIC)



JePPIX





Entry costs for different production models (1)

Vertical integrated fab

- Cleanroom cost >100 M€
- > 1 Mchips for chip cost < 100 €/chip

Custom foundry

cleanroom costs shared by all customers
custom process development cost > 3 M€
> 30,000 chips for chip cost < 100 €/chip</pre>



Entry costs for different production models (2)

Generic foundry

- Cleanroom costs shared by all customers
- Process development costs shared
- Process qualification costs shared
- Cost of shared infrastructure for large volumes: a few ∉mm²
- Entry cost reduction
 - R&D time shortened by dedicated software design kit with accurate models for the building blocks
 - R&D cost reduced by *Multi-Project wafer Runs* (MPR)
 - chip testing costs reduced by *building-block approach*
 - R&D cost < 300 k€, 1 trial < 100 k€ (interesting for SME's)
 - > 3000 chips for chip cost < 100 €/chip
 - > 300 chips for chip cost < 1000 €/chip
- Develop generic packaging and testing approaches





non-telecom applications



Optical Coherence Tomography



Fibre strain sensor for construction integrity monitoring



Skin analysis equipment

Compact Frequency comb-generators for metrology





UCSB, 7 Nov 2008 23/31

Outline

- Introduction
- Past / Moore's law in Photonics
- Future / 1 Generic Integration Technology
- Future / 2 Nanophotonic Integration Technology



Saturation?



Photonic Integration

UCSB, 7 Nov 2008 25/31



TU/e Technische Universiteit Eindhoven University of Technology

From analog to digital

Martin Hill et al., Nature, Vol. 432, 11 Nov. 2004, pp.206-209



Digital photonic flip-flop based on coupled micro-lasers

Dimensions Switching time Switching energy < 20 x 40 µm² < 15 ps < 6 fJ



Track 2: Metallic and Plasmonic lasers

A BREAKTHROUGH The world's smallest electrically injected laser (diameter 250 nm)

small active volume means low power and high speed

Martin Hill et al., Nature Photonics, October 2007



Latest Results for MIM structures

- Most devices from 80-300 nm worked pulsed at 250K
- For ~300 nm semiconductor core size room temperature (298K) operation (pulsed)
- Life time issues at higher temperatures
- Higher threshold current
- But, just beginning, not optimized
- Much room for improvement



Confidential





Photonic Integration

Photonic Integration

29/31 UCSB. 7 Nov 2008





- rectangular pillars 3 and 6 micron long •
- core width 80nm

Confidential

Record small MIM Devices







Potential



- Integration of more than 100,000 lasers on a chip
- Operating at speeds well beyond 1 THz

Superior to high-speed transistors for ultrafast signal processing



Complexity of InP Photonic ICs?





